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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 13

Application Number: 09/400,508
Filing Date: September 20, 1999
Appellant(s): ALLEE, DAREN

Mr. Louis H. Iselin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 15, 2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-16 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,078,194	Lee	6-2000
5,955,893	Chang et al.	9-1999

3,651,334	Thompson et al.	3-1972
5,602,494	Sundstrom	2-1997

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Lee (US PAT. 6,078,194). Lee shows and teaches all the elements and means of the claimed invention of the claim 1:

Lee teaches a logic gate (see Fig. 4(a) and 4(b)), comprising: a low noise current source (see 32) coupled between a first terminal of a voltage supply (see Vcc) and an output terminal (see OUT in Fig. 1), the low noise current source being capable of delivering a preselected voltage signal to the output terminal having a magnitude responsive to a first control signal (see PEN) relatively independent of the magnitude of the voltage on the first terminal of the voltage supply, and at least one switching element (see 36 and 38) coupled between the output terminal and a second terminal (see VTT) of the voltage supply, the switching element being capable of coupling the output terminal to the second terminal of the voltage supply in response to receiving a control signal (see A or B).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194).

Lee discloses the logic gate as set forth in claim 1 where the low noise current source includes a transistor (see 32) and a second transistor (see 34) whose gate is

connected to the source serially coupled between the first terminal of the voltage supply and the output terminal, the transistor having a gate capable of receiving the first control signal, but does not discloses the second transistor being a resistor.
However, it is well known in the art that the second transistor is configured as a diode and the diode configured transistor is recognized as equivalent to a resistor in this environment. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have replace the second transistor of Lee with a resistor for the purpose of reducing through current.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194) in view of Chang et al. (US PAT. 5,955,893).

Lee discloses the logic gate, as set forth in claim 1 but does not disclose the transistor is an intrinsic transistor.

However, Chang et al. discloses an intrinsic transistor (see 508 in Fig. 6) for the purpose of providing a transistor having a lower magnitude of threshold voltage.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to combine the transistor of Lee with the intrinsic transistor of Chang et al. because it would provide full voltage at the output terminal since the threshold voltage of the intrinsic transistor is lower than non-intrinsic transistor.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194) in view of Thompson et al. (US PAT. 3,651,334).

Lee discloses the logic gate, as set forth in claim 1 but does not disclose a capacitor coupled between the output terminal and the second terminal of the voltage supply.

However, Thompson et al. discloses a capacitor (see 28 in Fig. 1) coupled between the output terminal and the ground for the purpose of providing charging the output node.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to combine the logic gate of Lee with the capacitor of Thompson because it would provide a precharged voltage.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194) in view of Sundstrom (US PAT. 5,602,494).Lee discloses the logic gate, as set forth in claim 1 but does not disclose at least one clamping diode coupled between the output terminal and the second terminal of the voltage supply.

However, Sundstrom discloses a clamping diode (see 142 in Fig. 2) coupled between the output terminal and a second terminal for the purpose of providing input protection.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to combine the logic gate of Lee with the clamping diode of Sundstrom because it would provide input protection from an external terminal.

Apparatus claims 6-15 are essentially the same in scope as rejected apparatus claims 1-5 and 16 and are rejected similarly.

(11) Response to Argument

Appellant asserts numerous reasons as to why the rejection of claim 1 is inappropriate on pages 8-10.

Appellant asserts that claim 1 is not anticipated by Lee because Lee does not show each and every limitation recited in claim 1. In support of this, appellant notes that "Lee does not teach or fairly suggest controlling noise as with the present invention" (see Appeal Brief at p. 8). Appellant argument contends that Lee intends to show logic gates with reduced power when not in use. Indeed, Lee teaches logic gates with reduced power when not in use as well as a low noise current source, the transistor 32 in Fig. 4(a) of Lee. The transistor 32 inherently provides lower noise current compared to a simple coaxial resistor. The Examiner further notes that there is no basis to appellant's argument that claim 1 specifically and clearly recites "controlling noise" limitation. Claim 1 merely recites "a low noise current source".

Appellant further argues that "Lee does not teach the element of claim 1 of delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply" and the transistor 32 of Lee produces an output voltage that is very dependent on the supply voltage (see Appeal Brief at p. 9). However, the term, "relatively independent" is vague and presumes there is a relative dependency as well. The examiner notes that the control signal PEN of Lee, which

enables the transistor 32 is relatively dependent of the supply voltage, that is, the control signal PEN is relatively independent of the supply voltage.

Appellant argues Lee would be ineffective as an anticipatory reference under 35 U.S.C. § 102 in claim 1 when a n-type transistor is replaced with a p-type transistor. However, the examiner notes that there is no basis to appellant's argument the claim 1 specifically and clearly recites "n-type transistor" or "p-type transistor" limitation. Claim 1 merely recites " a low noise current source" instead.

Appellant goes on to argue that "Lee does not render claim 1 obvious" and the replacement of n-type transistor with p-type transistor having an inverter at the gate of the p-type transistor would cause significant misoperation and would be illogical (see Appeal Brief p. 10). However, the Examiner notes that replacing a n-type transistor 32 of Lee with a p-type transistor having an inverter at the gate of the p-type transistor would not cause the significant misoperation and would be art recognized equivalent circuits. It is well known in the art that the n-type transistor is turned on when a logic high signal is applied to the gate of the n-type transistor and the p-type transistor is turned on when a logic low signal is applied to the gate of the p-type transistor. When the PEN signal of Lee is a logic high and provide to an input of the inverter, the inverter inverts the PEN signal to a logic low signal. The inverted PEN signal, i.e. the logic low signal would turn on the p-type transistor and provides the current to the output node 100. Thus, such a replacement would produce the appropriate output signal and would provide a low noise current source that delivers a preselected voltage signal to the

output node having magnitude responsive to a control signal relatively independent of the supply voltage since the p-type transistor is enabled by the logic low signal.

Appellant argues that "any of Chang et al, Thompson et al., and Sundstrom remove the deficiency of Lee described above" with respect to claims 3, 4, and 5. However, the Examiner notes that Lee clearly shows all the limitation of claim 1 where the n-type transistor 32 provides lowers noise current source compared to a coaxial resistor and the transistor 32 delivers a preselected voltage signal to the output node having a magnitude responsive to a first control signal relatively independent of the supply voltage as discussed above.

Appellant goes on to argue that the rejection is vague with respect to rejection of claims 6-15 (see Appeal Brief p. 11). Appellant argues that "independent claim 6 includes an additional recitation to the current source having an intrinsic transistor". However, the intrinsic limitation of claim 6 has been rejected in the rejection of claim 3 which was obvious over Lee in view of Chang et al.,

claim 7 which includes the limitation of a resistor coupled with the intrinsic transistor has been rejected in the rejection of claims 2 and 3,

claim 8 which includes the limitation of a capacitor has been rejected in the rejection of claim 4,

claim 9 which includes the limitation of a clamping diode has been rejected in the rejection of claim 5,

claim 10 which includes the limitation of a p-type transistor has been rejected in the rejection of claim 16,

claim 11 which includes the limitation of a p-type transistor has been rejected in the rejection of claim 16,

claim 12 which includes the limitation of a resistor coupled with the p-type transistor has been rejected in the rejection of claim 2,

claim 13 which includes the limitation of an intrinsic transistor has been rejected in the rejection of claim 3,

claim 14 which includes the limitation of a capacitor has been rejected in the rejection of claim 4, and

claim 15 which includes the limitation of a clamping diode has been rejected in the rejection of claim 5.

Appellant goes on to argue that "Chang et al. adds nothing to further the Examiner's argument that "Lee neither discloses nor suggests that an intrinsic transistor could be used in a current source of a logic gate..." (see Appeal Brief p. 11). However, the examiner notes that Chang et al. discloses an intrinsic transistor for the purpose of providing a transistor having a lower magnitude of threshold voltage. It clearly would have been obvious to have implemented with an intrinsic transistor in the event the designer of the circuit needed slight different threshold voltage level.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

JHC
May 3, 2002

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